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A SYSTEM AND A METHOD FOR PLATING A CONDUCTIVE PATTERN

BACKGROUND OF THE INVENTION

In the solid state electronics industry, a plurality of components being active devices as well as passive devices are processed on a surface of a semiconductor wafer to form an integrated circuit. To form these integrated circuits metallization structures are requested both as a part of the aforementioned devices and to interconnect these devices. The formation of such metallization structures can include the plating of a conductive pattern, being part of a metallization structure and being formed at a first surface of a substrate, such as a wafer. Particularly this first surface can be the front side or the back side of the wafer.

One of the issues involved is the plating of this first surface of a substrate without exposing a second surface of a wafer, opposite to the first surface, to a plating solution. Particularly, exposure, even partly, would result in unwanted wetting, plating and/or corroding of other surfaces. Furthermore to be able to deposit a material by electroplating, the plating solution must be in contact with the first surface of the substrate comprising the conductive patterns to be plated and two electrically connectable electrodes have to be provided. Usually, the first electrode is immersed in the plating solution, while the second electrode has to be electrically connected to the conductive patterns to be plated. State-of-the-art plating techniques usually contact peripheral regions of the first surface of a substrate, comprising the conductive patterns to be plated. These peripheral contact regions are electrically connected to the second electrode as well as to the conductive patterns to be plated.

A problem is that often long metal lines are required to connect each conductive pattern to be plated with the contact in the peripheral region. Particularly, this is a problem when one wants to perform plating on wafer scale because the differences in distance between conductive patterns to be plated being located near the edges of the wafer and in the center of the wafer are huge. These differences are typically in the centimeter range. Consequently also the differences in resistance of the metal lines connecting the respective conductive patterns can be huge. This often results in a highly non-uniform plating process. All these metal connections between the conductive patterns to be plated and the peripheral regions can not be easily removed after the plating process and moreover, a lot of wafer-area is required to provide these connections thereby inhibiting dense integration.

Another problem is that the contact means in the peripheral regions are exposed to the plating solution. These contact means become parasitically plated and hav to be cleaned regularly. A further problem can arise if the contact means do not simultaneously can be used as sealing means, then extra sealing means are required. These sealing means should then be positioned between the contact means and the edges of the wafer in order to avoid leakage of the plating solution to another surface of the wafer. Consequently, this leads again to a further decrease of the available area of the wafer which can be plated.

DESCRIPTION OF THE INVENTION

In an aspect of the invention a plating system is disclosed for plating a plurality of conductive patterns formed at a surface of a substrate. A plating solution is applied on this surface and the exposure of other surfaces of the substrate to the plating solution is inhibited. A first electrode of the system is immersed in the plating solution while the second electrode is in contact with another surface of the substrate. The conductive patterns to be plated are removably electrically connected with the second electrode resulting in a uniform and selective deposition over the exposed surface of the substrate. Particularly, according to this aspect of the invention, a system is disclosed for plating at least one conductive pattern, said conductive pattern being positioned at a first surface of a substrate having at least a first surface and a second surface, said first surface being exposed to a plating solution, said system comprising:

a support with an electrically connectable electrode thereon;

a sealing element inhibiting the exposure of the second surface of the substrate to the plating solution; and

where said substrate is mountable on said support such that said electrode is in contact with said second surface of said substrate and wherein a contacting element to said first surface of said substrate is provided, said conductive pattern being removably electrically connected with said contacting element and said contacting element being electrically connected with said electrode. Particularly, the electrical connection between the contact element at the first surface of the substrate and the electrode at the second surface of the substrate can be a doped semi-conductive region of either an n-type conductivity or a p-type conductivity, or a metal via connection extending from the first surface to the second surface of the substrate. Furthermore, a metal contact can be provided at the second surface of the substrate. The aforementioned conductive patterns can be positioned at the first surface of the substrate, particularly, they can be positioned directly on the first surface of the substrate or on at least one dielectric layer formed on this first surface of the substrate.

In an embodiment of the invention a system is disclosed for plating a plurality of conductive patterns formed at a surface of a substrate. Each conductive pattern to be plated is removably electrically connected with a contact element contacting the substrate at the first surface of the substrate by a polysilicon conductor or an amorphous silicon conductor. Particularly, the conductive pattern is

positioned on a first die and the corresponding contact element is positi ned on a second die different from said first die. Preferably said second die is adjacent t said first die to keep the polysilicon or amorphous silicon conductor as short as possible to minimize the resistance of the connection. Consequently the plating can be performed in a substantially uniform manner.

In another embodiment of the invention a system is disclosed for plating a plurality of conductive patterns formed at a surface of a substrate, where at least a part of a conductive pattern and/or a contact element contacting the substrate at a first surface of a substrate is covered with a layer to inhibit plating said part. Particularly this layer can be a resist layer. By doing so the usually undesired plating of a contact element can be avoided.

The substrate can be a piece of a conductive material or a doped semi-conductive material. Particularly a silicon semiconductor wafer of a n-type or p-type conductivity can be used. The plating solution can be any commercially available plating solution. Of particular interest are plating solutions containing an metal, particularly a metal selected from a group comprising Ag, Cu, Au, Pt, Ti, Ni and Co. The conductive patterns are usually metal patterns. Particularly Al-containing or Cu-containing or Pt-containing patterns can be used.

In another aspect of the invention, a substrate is disclosed having at least a first surface and a second surface opposite to said first surface, said first surface being exposable to a plating solution, said substrate comprising

a conductive pattern being positioned at said first surface of a substrate;

a contact element contacting the substrate at the first surface of the substrate said conductive pattern being removably electrically connected by a polysilicon or an amorphous silicon conductor with said contact element and said contact element being electrically connected with said second surface.

In a further aspect of the invention, a method is disclosed for plating at least one conductive pattern formed at a surface of a substrate, said substrate having at least a first surface and a second surface, said method comprising the steps of:

placing the substrate on an electrode being part of a plating holder such that said second surface of said substrate is in contact with said electrode and said conductive pattern is removably electrically connected to said conductive pattern; and

applying a plating solution on said first surface of said substrate thereby inhibiting exposure of said second surface to said plating solution.

In another embodiment of the invention, a plating solution is disclosed wherein said electrode and said conductive pattern are removably electrically connected by forming a polysilicon or an amorphous silicon conductor to removably connect said conductive pattern with a contact element, said contact element being formed on the first surface of the substrate and contacting the substrate, and by providing an electrical connection between said contact element and said electrode. The resistance of the electrical connection between the contact element and the electrode is substantially independent of the location of the contact element at the first surface of the substrate. Therefore, to achieve a high degree of uniformity over the substrate of the plating process, preferably the length of the polysilicon or the amorphous silicon conductor should be kept as short as possible. On the other hand, one has to be able to easily cut the connection provided by the silicon or the amorphous silicon conductor after the plating process. Therefore, preferably, the conductive pattern is positioned on a first die and said contact element is positioned on a second die different from said first die. By doing so, the connection can by cut by dicing the substrate. More preferably, said first and said second die are adjacent dies.

In another embodiment of the invention a method is disclosed, wherein prior to applying the plating solution, a resist layer is deposited on said conductive pattern and patterned in order to create at least one covered area an at least one uncovered area, said uncovered area being exposable to said plating solution.

In an embodiment of the invention, as an example, a system and a method for selectively electroplating a plurality of platinum patterns is disclosed. The platinum patterns to be plated are formed on the front side of a silicon wafer with a p type conductivity. Each aluminum pattern (fig.1) to be plated is connected by means of a polysilicon line to an aluminum contact element contacting the p-type substrate region of the wafer at the front side of the wafer. This contact element is positioned on an adjacent die. The polysilicon line is isolated from the wafer by means of at least one dielectric layer. The polysilicon line extends over a dicing line (fig. 2). Accordingly, all platinum patterns to be plated are electrically connected to the back side of the wafer which can be provided with an aluminum metal contact.

Before applying a plating solution, the wafer is placed on a support with an electrically connectable electr de thereon such that there is an electrical between the back side of the wafer and the electrode. This support is a part of a wafer holder designed for plating purposes. During the plating process, the plating solution is brought in contact with the front side of the wafer, while the backside is sealed by means of a sealing element being part of the aforementioned wafer holder (fig. 3). Particularly, this sealing element is a sealing ring which inhibits the exposure of the backside of the substrate to the plating solution The backside of the wafer is electrically connected with a backside electrode of the same size. By immersing a similar electrode as counter electrode in the plating solution, a homogeneous electrical field can be created. The plating process is galvanostatic, e.g. the current is held constant by regulating the potential between the backside and the counter electrode. According to the example, silver is electroplated and an alkaline silver solution is used as plating solution. A negative potential is applied at the backside electrode.

In order to avoid plating of the aluminum contact elements at the front side of the substrate, a positive photoresist layer (AZ4562 from Hoechst) is used to cover those areas where no plating may occur.

Finally, the wafers are stripped and diced. Figure 4 and figure 5 show respectively a cross-section and top view of the polysilicon lines. By dicing over the polysilicon lines, the electroplated structures are disconnected from the respective contact elements.

By using the substrate as a contacting layer for an electrode, the electrical resistance between the areas to be plated and the electrical contact point is for all plated structures substantially the same, particularly if the length of the polysilicon lines is kept sufficiently short and the specific resistance of the polysilicon line is sufficiently low. This length has to be sufficiently short to assure that the resistance of the polysilicon lines has a negligible contribution to the total resistance of the connection between the conductive pattern and the backside of the wafer. Accordingly, the uniformity of the plating process is increased or another words, the homogeneity of the deposited thickness of the plated material over the complete wafer is increased. In the example, the plated material is silver.

By dicing over the polysilicon lines, the individual electroplated patterns are disconnected one from the other and are no longer in contact with the substrate. By using polysilicon or amorphous silicon lines extending over the dicing lines, the risk to create electroplated patterns, being short-circuited to the substrate after dicing is reduced. If metal lines or leads would be used to provide the connection to the

contact elements, then the electroplated patterns can still be in contact with the substrate after dicing due to metal shavings or residues.

The same plating system and method as defined according the present invention can be used for electrochemical chloridation on wafer scale provided that a different solution is used and a positive potential is applied at the backside electrode instead of a negative potential. Of particular interest is the electrochemical chloridation of silver. The electrochemical chloridation of bulk silver electrodes (wires) can be used for producing standard reference electrodes. An advantage is that the quality of the AgCl layer formed by using electrochemical chloridation is better than by using a chemical chloridation. So, according to the present invention, Ag/AgCl reference electrodes on wafer scale can be formed by using electroplated silver and electrochemically chloridized silver chloride.

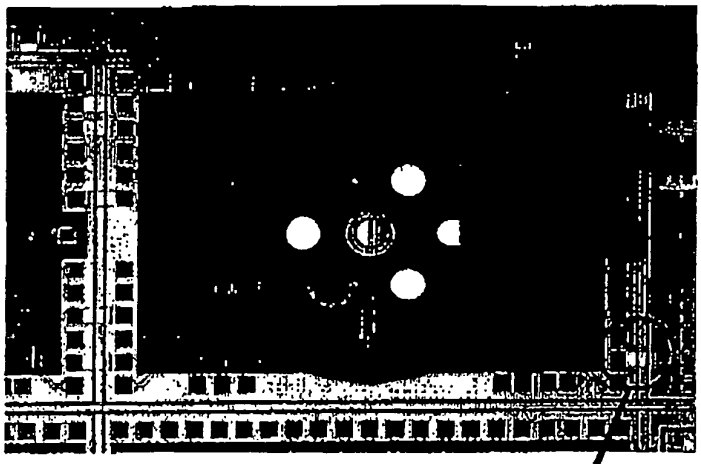


Figure 1: Structures to be plated, are connected to polysilicon stripes which cross the dicing line

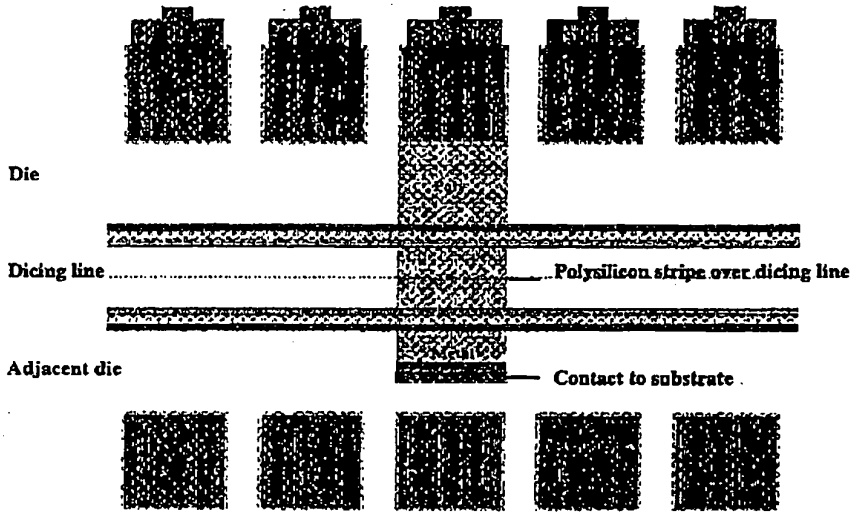


Figure 2: Polysilicon stripe with substrate contact on adjacent die

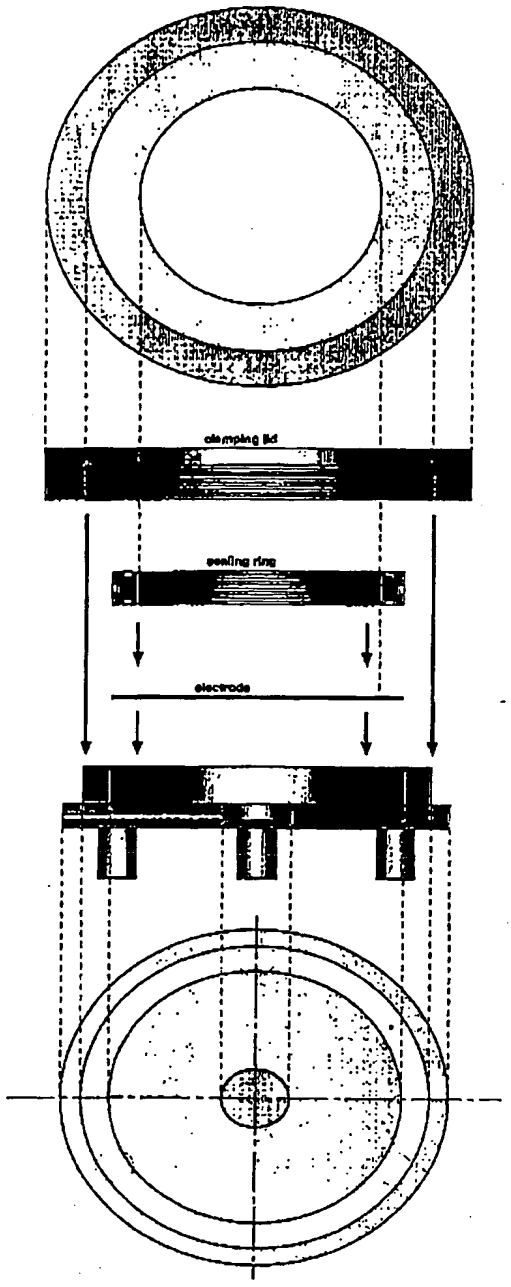
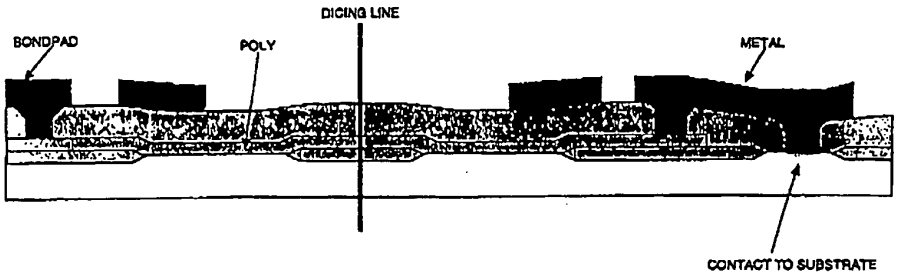


Figure 3: Plating holder with backside contact

Figure 4 and figure 5 show respectively a cross-section and top view of the polysilicon stripes. By dicing over the polysilicon stripe, the electroplated structures are disconnected from the substrate contact.



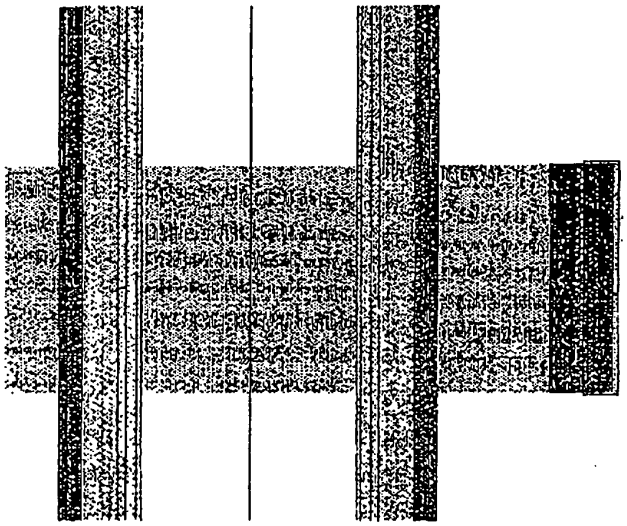


Figure 4: Cross-section and top view of a polysilicon stripe over the dicing line

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